

DESCRIPTION

The MP20051 is a low-dropout linear regulator that supplies up to 1A current with a 140mV dropout voltage. The externally-adjustable output voltage has a range of 0.8V to 5V from an input voltage of 2.5V to 5.5V.

An internal PMOS pass element allows for a low 110µA ground current, making the MP20051 suitable for battery-powered devices. Other features include low-power shutdown, and short-circuit and thermal protection. The MP20051 is available in 3mm x 3mm 8-pin QFN and SOIC8E packages.

FEATURES

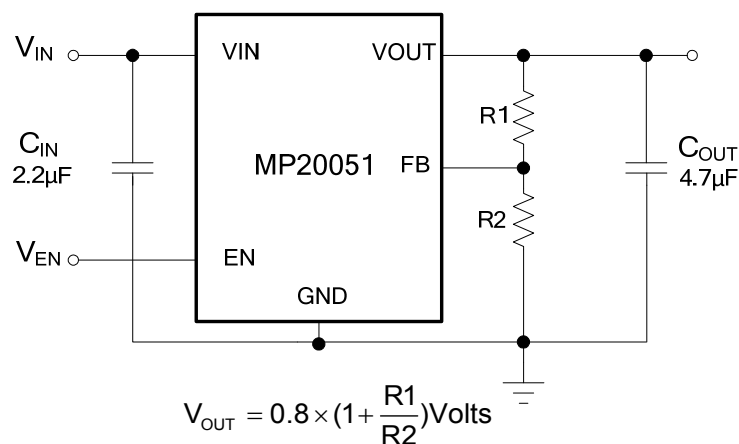
- Up to 1A Output Current
- Low 140mV Dropout at 1A
- Low 110µA Ground Current
- Output Voltage Available from 0.8V to 5V
- Low Noise: 13µV_{RMS} typical (10Hz to 100kHz)
- 63dB PSRR @1kHz
- Stable with Ceramic Capacitor
- Excellent Load/Line Transient Response
- Current Limiting and Thermal Protection
- Available in 3mm x 3mm 8-pin QFN and SOIC8E Packages

APPLICATIONS

- Notebook Computers
- Cordless Telephones
- Cellular Phones
- Wireless Communication Equipment
- Hand-Held Instruments

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TYPICAL APPLICATION



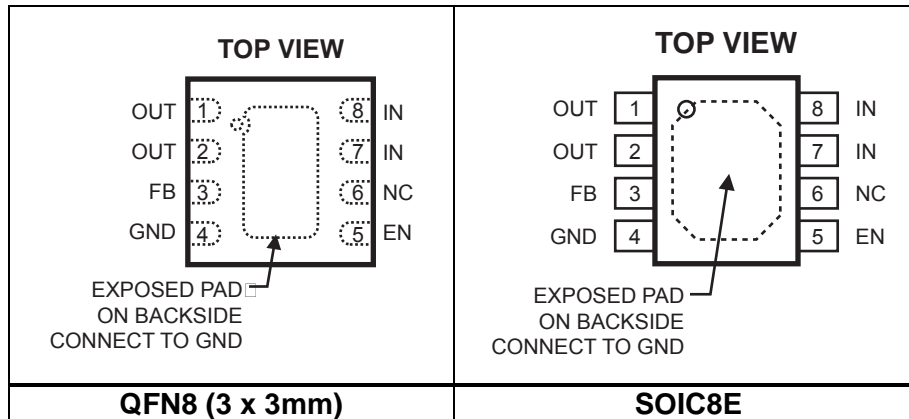
ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T _A)
MP20051DQ*	QFN8 (3 x 3mm)	ABR	-40°C to +85°C
MP20051DN**	SOIC8E	MP20051	

* For Tape & Reel, add suffix -Z (e.g. MP20051DQ-Z);
 For RoHS Compliant Packaging, add suffix -LF (e.g. MP20051DQ-LF-Z)

** For Tape & Reel, add suffix -Z (e.g. MP20051DN-Z);
 For RoHS Compliant Packaging, add suffix -LF (e.g. MP20051DN-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

V _{IN} , EN, FB to GND	-0.3V to +6V
OUT to GND	-0.5V to (V _{IN} + 0.5V)
Continuous Power Dissipation	(T _A =25°C) ⁽²⁾
QFN8 (3x3mm).....	2.0W
SOIC8E	2.0W
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10sec).....	260°C

ESD SUSCEPTIBILITY⁽³⁾

HBM (Human Body Mode).....	2kV
MM (Machine Mode)	200V

Recommended Operating Conditions ⁽⁴⁾

Supply Input Voltage.....	2.5V to 5.5V
Enable Input Voltage	0V to 5.5V
Operating Junction Temp. (T _J). -40°C to +125°C	

Thermal Resistance ⁽⁵⁾ θ_{JA} θ_{JC}

QFN8 (3x3mm)	50	12 ... °C/W
SOIC8E	50	10 ... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Devices are ESD sensitive. Handling precaution recommended.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN}=V_{OUT}+0.5V$ or $V_{IN}=2.5V$, $EN=V_{IN}$, Typical values are at $T_A=25^\circ C$, unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Input Voltage		2.5		5.5	V
Input Under Voltage Lockout	V_{IN} rising	1.95		2.25	V
Hysteresis of UVLO			160		mV
FB Voltage	$V_{OUT}=0.8V$, $I_{OUT}=1mA$	0.784	0.8	0.816	V
Output Voltage Accuracy	$I_{OUT}=1mA$, $T_A=25^\circ C$	-2		2	%
	$I_{OUT}=1mA$, $-40 \leq T_A \leq 85^\circ C$	-3		3	
Maximum Output Current	Continuous, $V_{IN} \geq 2.5V$, $V_{OUT}=2.5V$	1			A
Short-Circuit Current Limit	$V_{OUT}=0$, $V_{IN} \geq 2.5V$		1.6		A
In-Regulation Current Limit	$V_{OUT}=2.5V$, V_{OUT} within 4% of normal output voltage $V_{IN}=5.5V$	1.4	2.2	3.0	A
Ground Current	$I_{OUT}=0.1mA$, $V_{OUT}=2.5V$		110		μA
	$I_{OUT}=1A$, $V_{OUT}=2.5V$			600	
Dropout Voltage ⁽⁶⁾	$I_{OUT}=1A$, $V_{OUT}=2.5V$		140	280	mV
	$I_{OUT}=750mA$, $V_{OUT}=2.5V$		105	210	
	$I_{OUT}=500mA$, $V_{OUT}=2.5V$		70	140	
Line Regulation ⁽⁷⁾	$V_{OUT}=2.5V$, V_{IN} from $V_{OUT}+0.5V$ to $5.5V$, $I_{OUT}=100mA$,	-0.15		0.15	%/V
Load Regulation ⁽⁸⁾	I_{OUT} from 100mA to 1A, $V_{OUT}=2.5V$		0.3		%
Output Voltage Noise	$I_{OUT}=100mA$, f ranges from 10Hz to 100kHz	$V_{OUT}=1.1V$	13		μV_{RMS}
		$V_{OUT}=3.3V$	35		
		$V_{OUT}=5V$	55		
PSRR	$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$	f=100Hz	65		dB
		f=1kHz	63		
		f=10kHz	63		
		f=1MHz	33		
Shutdown Supply Current	$V_{IN}=+5.5V$		0.2		μA
EN Pin Current , Enabled	$V_{IN}=V_{EN}=+5.5V$		0.2		μA
Feedback Pin Current	$V_{IN}=+5.5V$, $V_{FB}=6V$		0.02		μA
Startup Time	$V_{OUT(NOM)}=2.5V$, $C_{OUT}=4.7\mu F$, $V_{OUT}=0\%$ to $90\%V_{OUT(NOM)}$		45		μs
EN PIN Threshold	EN Logic High	1.5			V
	EN Logic Low			0.4	
Thermal Shutdown Temperature	Typical thermal hysteresis = $20^\circ C$		150		$^\circ C$

Notes:

6) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

$$7) \text{ Line Regulation} = \frac{|V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}|}{[V_{IN(MAX)} - V_{IN(MIN)}] \times V_{OUT(NOM)}} \times (\% / V)$$

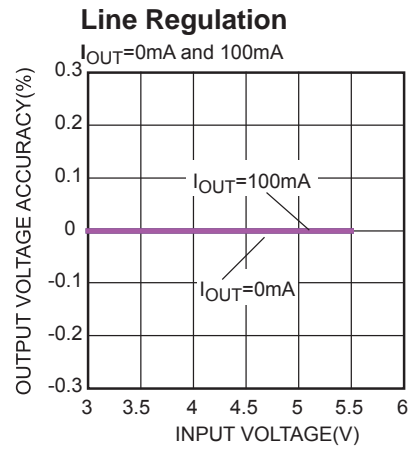
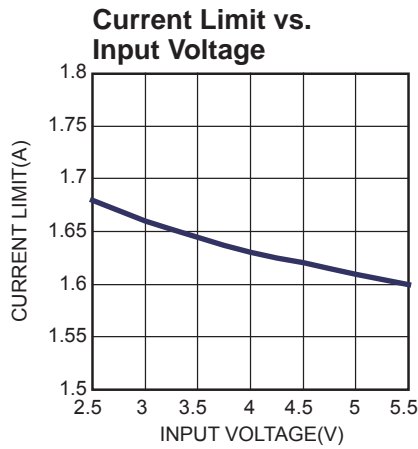
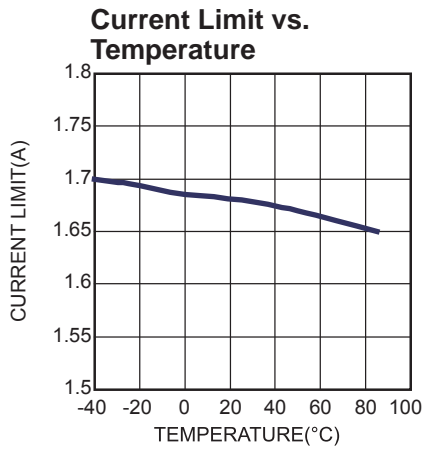
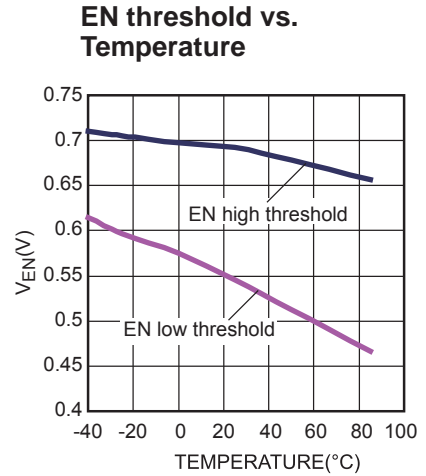
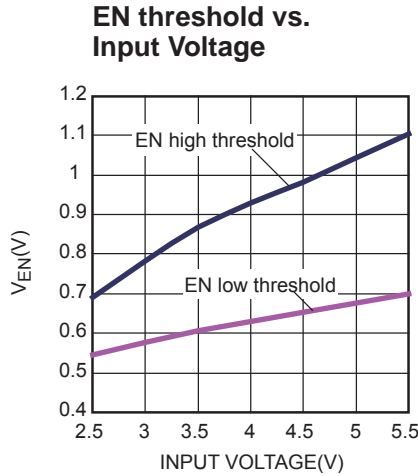
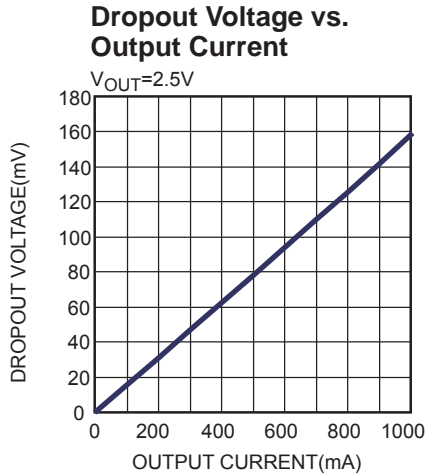
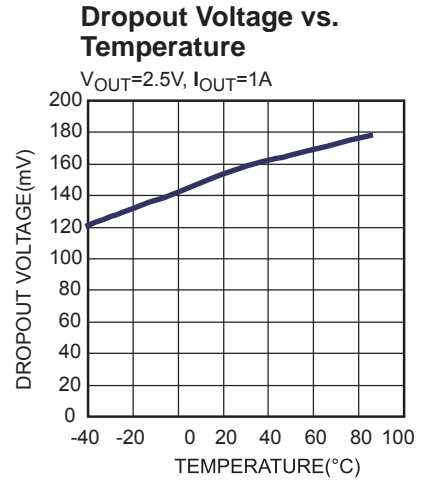
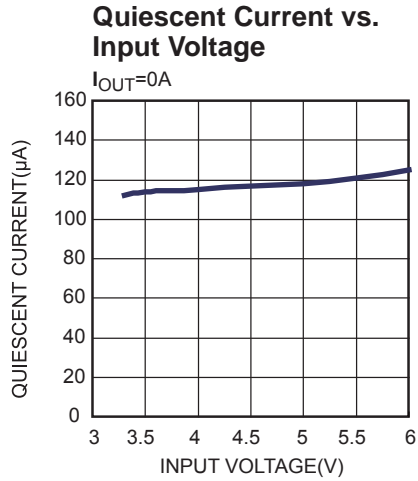
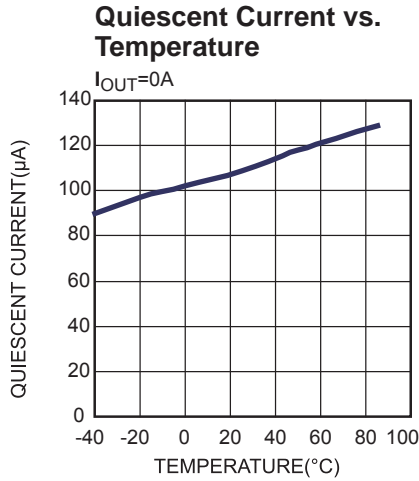
$$8) \text{ Load Regulation} = \frac{|V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}|}{V_{OUT(NOM)}} \times (\%)$$

PIN FUNCTIONS

Pin #	Name	Pin Function
1, 2	VOUT	Regulator output. Bypass with a standard 4.7 μ F ceramic capacitor to GND. Connect all the pins together externally.
3	FB	Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V.
4	GND Exposed pad	Ground. Connect exposed pad to GND plane for optimal thermal performance.
5	EN	Regulator Enable Control Input. Drive EN above 1.5V to turn on the MP20051. Drive EN below 0.4V to turn it off. Do not float the EN pin.
6	NC	No Connection. Leave this NC pin open.
7, 8	VIN	Regulator Input. Supply voltage ranges from 2.5V to 5.5V. Bypass with 2.2 μ F capacitor. These pins must be externally connected for proper operation even if they are internally connected.

TYPICAL PERFORMANCE CHARACTERISTICS

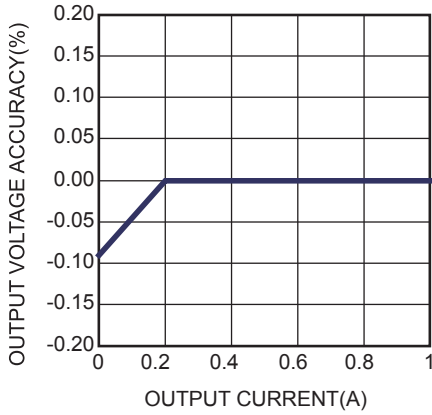
$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 4.7\mu F$, $T_A = 25^\circ C$, unless otherwise noted.



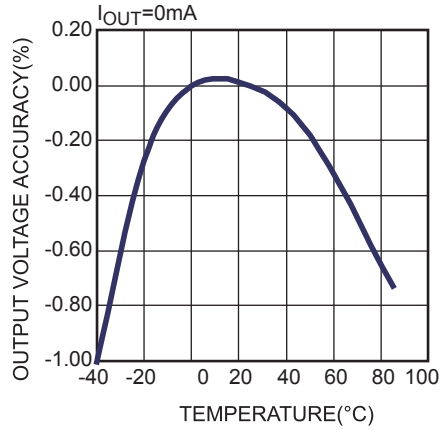
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $C_{IN}=2.2\mu F$, $C_{OUT}=4.7\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

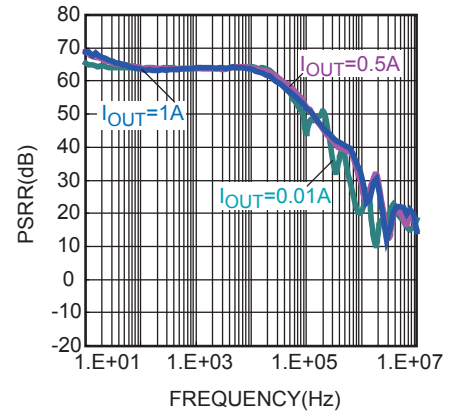
Load Regulation



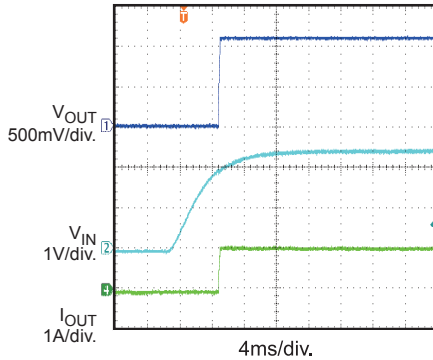
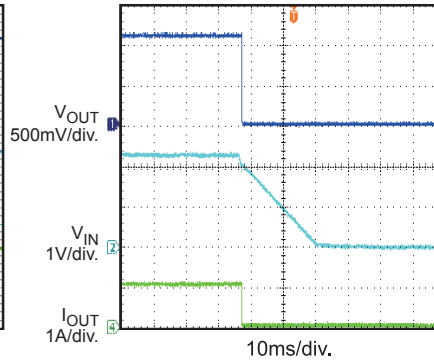
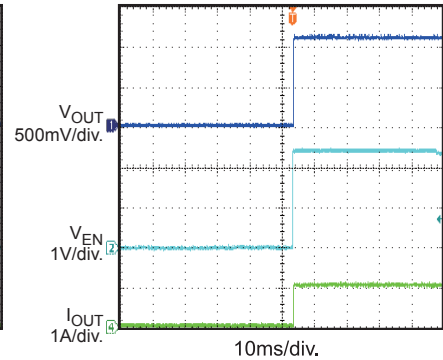
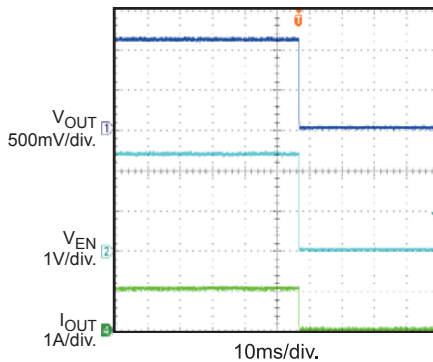
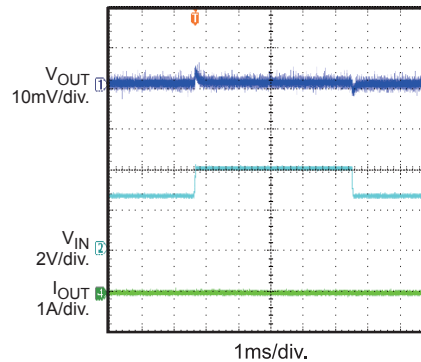
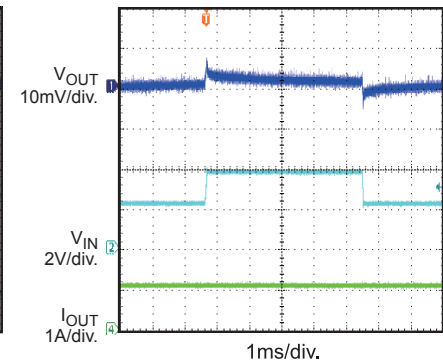
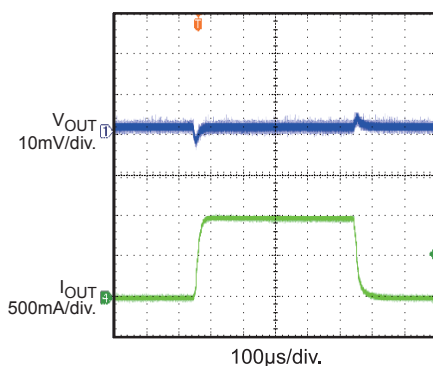
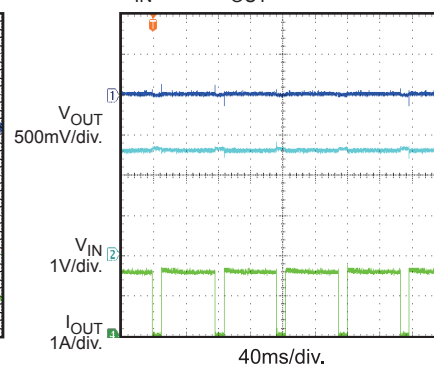
Output Voltage Accuracy vs. Temperature



PSRR Vs. Frequency



TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 4.7\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

Input Power Start Up
 $V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$,
with Resistor Load

Input Power Shutdown
 $V_{IN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$,
with Resistor Load

EN Start Up
 $V_{EN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$,
with Resistor Load

EN Shutdown
 $V_{EN} = 2.5V$, $V_{OUT} = 1.1V$, $I_{OUT} = 1A$,
with Resistor Load

Line Transient
 $V_{IN} = 2.5V$ to $4V$, $V_{OUT} = 1.1V$,
 $I_{OUT} = 10mA$, with Resistor Load

Line Transient
 $V_{IN} = 2.5V$ to $4V$, $V_{OUT} = 1.1V$,
 $I_{OUT} = 1A$, with Resistor Load

Load Transient
 $V_{IN} = 2.5V$, $V_{OUT} = 1.1V$,
 $I_{OUT} = 10mA$ to $1A$, with Resistor Load

**Over Current Protection
Steady State**
 $V_{IN} = 2.5V$, $V_{OUT} = 1.1V$


FUNCTIONAL BLOCK DIAGRAM

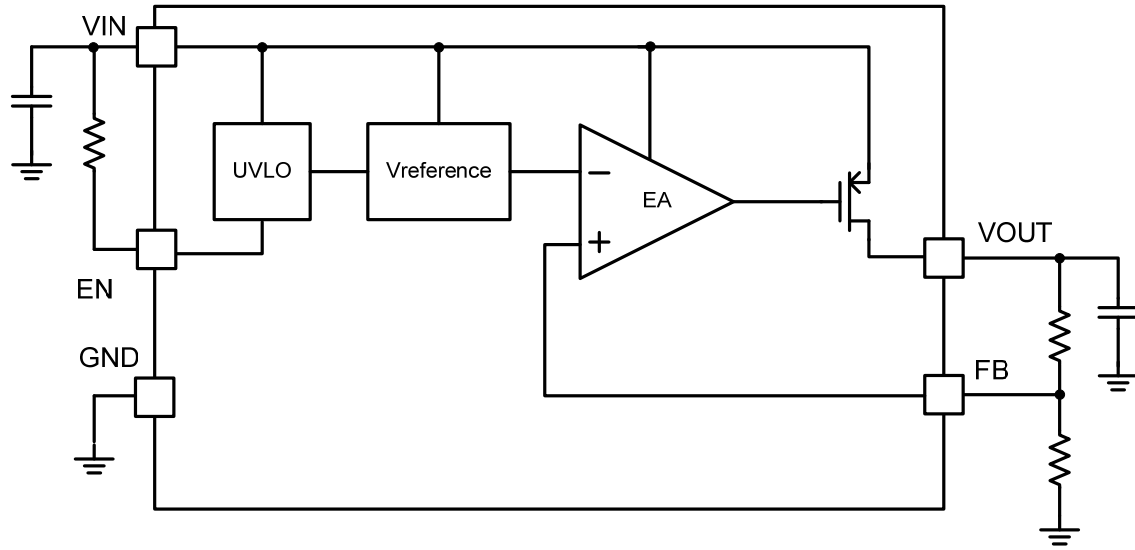


Figure 1—Functional Block Diagram

OPERATION

The MP20051 is a low-dropout linear regulator that can supply up to 1A current, which makes it suitable for very low voltage, low quiescent, low noise, and high PSRR applications such as wireless LAN transceivers, notebook computers, smartphones, and other low-power electronics.

The MP20051 uses an internal PMOS as the pass element and includes both thermal shutdown and an internal current-limiting circuit.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage of MP20051 is only 140mV.

Shutdown

The MP20051 can be switched ON or OFF by a logic input at the EN pin: Logic high turns the regulator on and logic low turns it off. Tie the EN pin to VIN if the application does not require the shutdown feature. Do not float the EN pin.

Current Limit

The MP20051 includes a current limit structure that monitors and controls the PMOS gate voltage to limit the guaranteed maximum output current to 1.6A.

Thermal Protection

Thermal protection turns off the PMOS when the junction temperature exceeds 150°C, allowing the IC to cool. When the IC's junction temperature drops by 20°C, the PMOS will turn on again. Thermal protection limits total power dissipation in the MP20051. For reliable operation, limit the junction temperature to a maximum of 125°C.

Load-Transient Considerations

The output response of the load-transient consists of a transient response and DC shift—the MP20051's excellent load regulation effectively limits the DC shift. The output voltage transient depends on the output capacitor's value and ESR. Increasing the capacitance and decreasing the ESR will improve the transient response.

APPLICATION INFORMATION

Setting the Output Voltage

The MP20051 has an externally-set output voltage with a range of 0.8V to 5V given a 2.5V to 5.5V input. Set the output voltage using a resistive voltage divider from the output voltage to the FB pin. The result of the voltage divider at the FB pin is:

$$V_{FB} = V_{OUT} \frac{R2}{R1 + R2}$$

Where V_{FB} is the feedback threshold voltage ($V_{FB} = 0.8V$), and V_{OUT} is the output voltage. Thus the output voltage is:

$$V_{OUT} = 0.8 \times \frac{R1 + R2}{R2}$$

$R2$ can go as high as 100k Ω , but typical applications use 10k Ω . After selecting $R2$, $R1$ is determined by:

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

For example, for a 1.1V output voltage, $R2$ is 10k Ω , and $R1$ is 3.75k Ω . You can select a standard 3.75k Ω ($\pm 1\%$) resistor for $R1$.

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature differential between the junction and ambient air, and the rate of air flow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

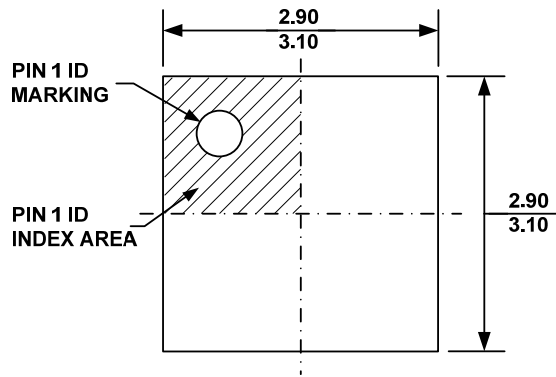
Where $(T_{Junction} - T_{Ambient})$ is the temperature differential between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connecting the exposed GND pad to a large ground pad or plane helps to channel away heat.

Output Capacitor Selection

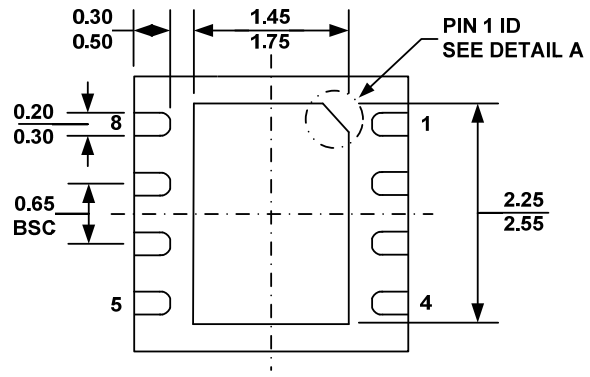
The MP20051 is specifically designed to work with a standard ceramic output capacitor to save space and improve performance. Use a 4.7 μ F ceramic capacitor for most applications. Larger output capacitors will improve load transient response and reduce noise at the cost of increased size.

PACKAGE INFORMATION

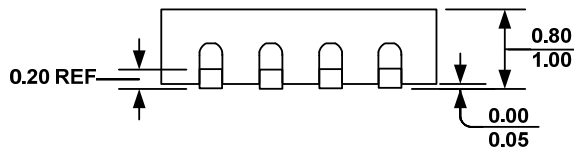
QFN8 (3×3mm)



TOP VIEW

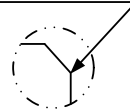


BOTTOM VIEW

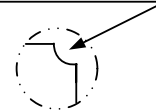


SIDE VIEW

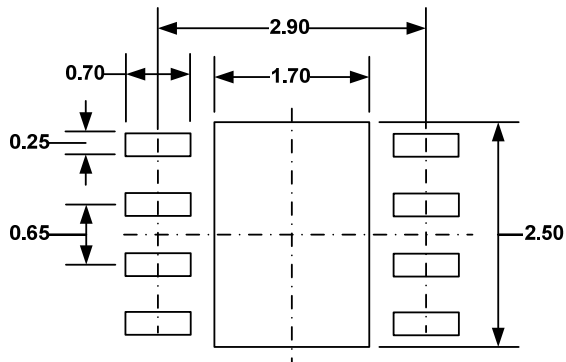
PIN 1 ID OPTION A
0.30x45° TYP.



PIN 1 ID OPTION B
R0.20 TYP.



DETAIL A

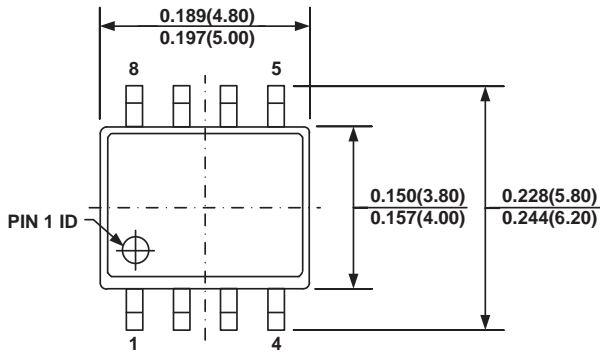


RECOMMENDED LAND PATTERN

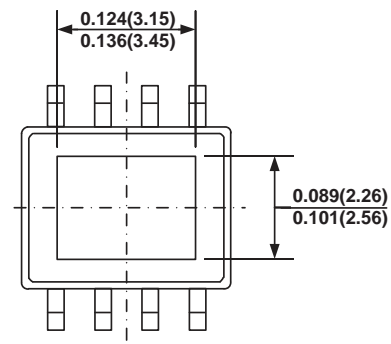
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEEC-2.
- 5) DRAWING IS NOT TO SCALE.

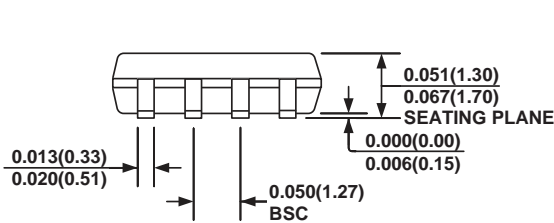
SOIC8E



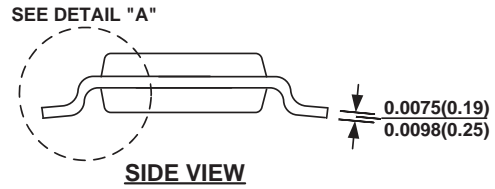
TOP VIEW



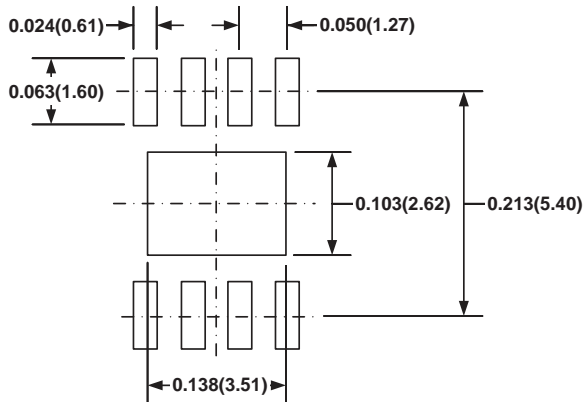
BOTTOM VIEW



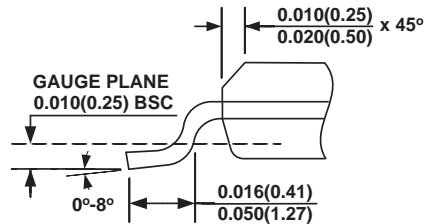
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

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